The following is a complete listing of all claims in the application, with an indication of the status of each:

Listing of claims:

1. (currently amended) A multichip circuit module having a main circuit board, at least one carrier substrate mounted on the main circuit board and which is in electrical contact with the main circuit board, and at least one semiconductor chip on the carrier substrate which is in electrical contact with the carrier substrate, wherein

the carrier substrate has at least one cavity on a mounting surface to accommodate said at least one semiconductor chip, the carrier substrate having a plurality of layers with conductor tracks extending transversely through said plurality of layers and terminating in conductor contacts on said mounting surface,

connecting contacts for associated bumps of said at least one semiconductor chip are provided in said at least one cavity,

the at least one semiconductor chip being mounted on the connecting contacts by using the associated bumps in a flip-chip technique, and

the mounting surface of the carrier substrate being applied to a contact surface of the main circuit board ~~and the mounting surface of the carrier substrate wherein the carrier substrate has many layers with conductor tracks extending transversely through a plurality of layers, and~~ via a filling material that provides i) a heat dissipation path from ~~makes contact with a rear of~~ said at least one semiconductor chip in said at least one cavity to said circuit board and ii) electrical connection between said conductor contacts and

corresponding contacts on said circuit board, without enclosing the connecting contacts and bumps.

2. (previously presented) The multichip circuit module as claimed in claim 1, wherein the filling material is an anisotropically conductive material.

3. (previously presented) The multichip circuit module as claimed in claim 1 wherein the filling material does not fill the interspaces of the at least one cavity completely.

4. (currently amended) The multichip circuit module as claimed in claim 1 wherein the conductor tracks of the carrier substrate are led to the mounting surface and are connected electrically and mechanically to conductor tracks of the main circuit board, and wherein said filling material provides insulation within the filling material between said conductor contacts and encapsulation of said at least one semiconductor chip, thereby providing for the simultaneous carrying of signals, dissipation of heat, encapsulation and shielding.

5. (previously presented) The multichip circuit module as claimed in claim 1 further comprising a planar antenna arrangement on an underside of the carrier substrate, which is opposite the mounting surface.

6. (previously presented) The multichip circuit module as claimed in claim 1 wherein the carrier substrate is a multilayer ceramic.

7. (currently amended) A method for production of multichip circuit modules having a main circuit board, at least one carrier substrate mounted on the main

circuit board and which is in electrical contact with the main circuit board, and at least one semiconductor chip on the carrier substrate which is in electrical contact with the carrier substrate, wherein

the carrier substrate has at least one cavity on a mounting surface to accommodate said at least one semiconductor chip, the carrier substrate having a plurality of layers with conductor tracks extending transversely through said plurality of layers and terminating in conductor contacts on said mounting surface,

connecting contacts for associated bumps of said at least one semiconductor chip are provided in said at least one cavity,

the at least one semiconductor chip being mounted on the connecting contacts by using the associated bumps in a flip-chip technique, and

the mounting surface of the carrier substrate being applied to a contact surface of the main circuit board ~~and the mounting surface of the carrier substrate wherein the carrier substrate has many layers with conductor tracks extending transversely through a plurality of layers, and~~ via a filling material that provides i) a heat dissipation path from ~~makes contact with a rear of~~ said at least one semiconductor chip in said at least one cavity to said circuit board and ii) electrical connection between said conductor contacts and corresponding contacts on said circuit board, without enclosing the connecting contacts and bumps, having the following steps:

a) letting the at least one semiconductor chip into cavities provided for semiconductor chips on a mounting surface of the carrier substrate;

b) mounting the at least one semiconductor chip by making contact with the bumps of the at least one semiconductor chip to connecting contacts in the cavities using a flip-chip technique;

c) applying a layer of filling material to the contact surface of the main circuit board; and

d) applying the carrier substrate having the mounting surface to the contact surface of the main circuit board.

8. (previously presented) The method as claimed in claim 7 wherein said applying a layer of filling material step is performed by application of an anisotropically conductive filling material to the contact surface.

9. (previously presented) The method as claimed in claim 7 wherein said applying a layer of filling material step includes application of the filling material in a layer thickness which is matched in such a way that interspaces of the cavities are not filled completely with the filling material.

10. (previously presented) The method as claimed in claim 7 further comprising the step of electrically connecting the conductor tracks, which extend transversely through a plurality of layers of the carrier substrate and are led to the mounting surface to conductor tracks of the main circuit board.

11. (previously presented) The method as claimed in claim 7 wherein the steps are performed in a gas atmosphere in order to enclose gas in the cavities.

12. (previously presented) The multichip circuit module of claim 2 wherein said anisotropically conductive material is selected from the group consisting of an anisotropically conductive paste and an anisotropically conductive film.

13. (previously presented) The multichip circuit module as claimed in claim 2 wherein the filling material does not fill the interspaces of the at least one cavity completely.

14. (previously presented) The multichip circuit module as claimed in claim 6 wherein said multilayer ceramic is a low-temperature co-fired ceramic (LTCC).

15. (previously presented) The method as claimed in claim 7 wherein said anisotropically conductive filling material is a paste or a film.

16. (previously presented) The method as claimed in claim 8 wherein said applying a layer of filling material step includes application of the filling material in a layer thickness which is matched in such a way that interspaces of the cavities are not filled completely with the filling material.

17. (previously presented) The method as claimed in claim 8 wherein the steps are performed in a gas atmosphere in order to enclose gas in the cavities.

18. (previously presented) The method as claimed in claim 9 wherein the steps are performed in a gas atmosphere in order to enclose gas in the cavities.

19. (previously presented) The method as claimed in claim 10 wherein the steps are performed in a gas atmosphere in order to enclose gas in the cavities.